

VDIC ASYNCHRONOUS STATIC RAM

VDSR16M08XS44XX4C12 USER MANUAL

Version : A0

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VDIC-SRAM

HIGH-SPEED 5.0V 2M × 8 bit

ASYNCHRONOUS STATIC RAM

1 Description

The VDSR16M08XS44XX4C12 is a high-speed access time, high-density Static Random Access Memory with 16Mbit. Manufactured with VDIC Very Dense SIP technology, this block is stacked by four SRAM chips employing CMOS process. It is organized as 2M×8bit wide data interface .The chip can be selected separately with dedicated #CS.

Low interconnect parasitic capacitance of the stacking technology, by reducing the connection length, allows this SRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.

The VDSR16M08XS44XX4C12 is available in a 44-pin SOP package.

2 Features

- High-speed access time: 12ns
- TTL compatible inputs and outputs
- Organized as 2M x 8-bit
- Single +5 ± 0.5V power supply
- Fully Static Operation
 - No clock or refresh required
- Three state Outputs.
- Centre Power/Ground Pin Configuration
- Available Temperature Range:
 - 0°C to 70°C
 - 40°C to +85°C
 - 55°C to +125°C

3 Block Diagram

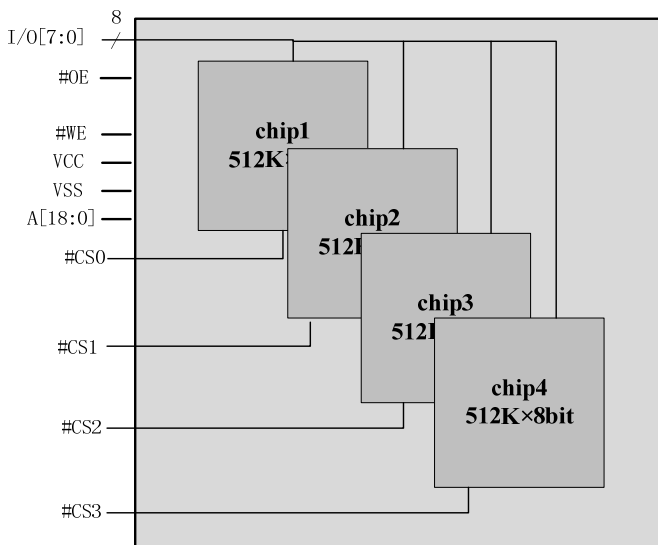


Figure 1 Block diagram

4 Pin Descriptions

Pin Id	Pin #	Pin Id
#CS2	1	44
#CS1	2	43
A0	3	42
A1	4	41
A2	5	40
A3	6	39
A4	7	38
#CS0	8	37
I/O0	9	36
I/O1	10	35
VCC	11	34
VSS	12	33
I/O2	13	32
I/O3	14	31
#WE	15	30
A5	16	29
A6	17	28
A7	18	27
A8	19	26
A9	20	25
#CS3	21	24
NC	22	23
		NC
		VSS

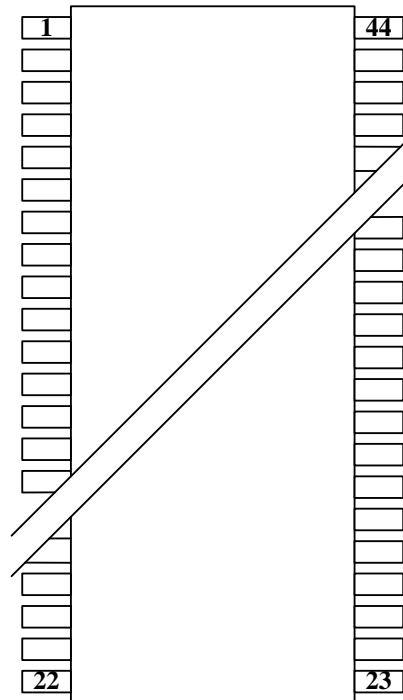


Figure 1 Pin configuration

Table 1 Pin description

Pin	Name	Function
#CS0~#CS3	chip select	Chip Enable Input
A0 ~ A18	Address	Address Inputs
#WE	Write enable	Write Enable Input
#OE	Output enable	Output Enable Input
I/O0~I/O7	Data input/output	Data inputs/outputs 8-bit wide bus
Vcc/Vss	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	This pin is recommended to be left No Connection on the device.

5 Command Operation

5.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Parameter	Symbol	Maximum ratings	Unit
Voltage on Vcc supply relative to Vss	VCC	-0.5 ~ VCC+0.5	V
Voltage on any pin relative to Vss	V _{IN}	-0.5 ~ VCC+0.5	V
Power Dissipation	P _D	1.4	W
Thermal Resistance Junction to Case	R _{J-C}	<20	°C/W
Manual Soldering Temperature Range	T _M	+250 ~ +280	°C
Reflow Soldering Temperature	T _{SOL}	215	°C
Operating Temperature Range	T _{OPR}	-55 ~ +125	°C
Storage Temperature Range	T _{STG}	-65 ~ +150	°C

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VCC	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.0	—	VCC+0.5	V
Input low voltage	V _{IL}	-0.5	—	0.8	V

5.3 DC Electrical Characteristics

Table 4 DC characteristics

Parameter	Symbol	TEST CONDITIONS	Min	Max	Unit
Output voltage low level	V _{OL}	VCC=4.5V, I _{OL} = 4mA	—	0.4	V
Output voltage high level	V _{OH}	VCC=4.5V, I _{OH} = -4.0mA	2.4	—	V

6 TYPICAL APPLICATION

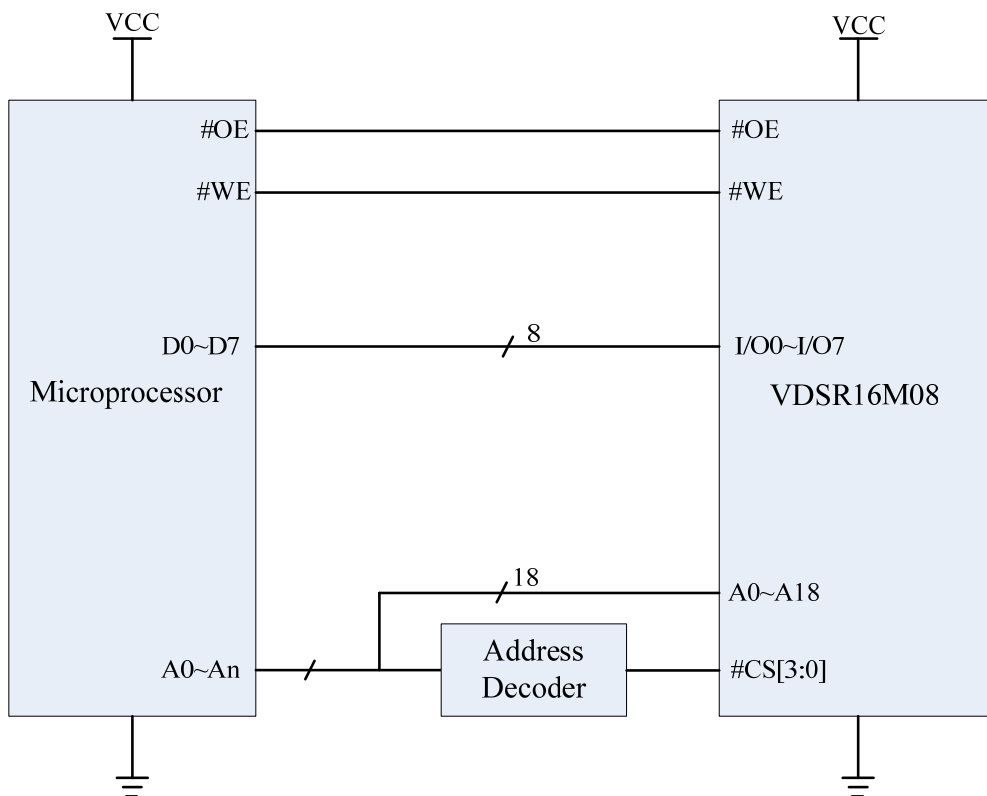


Figure 2 Typical application

7 Ordering Information

1	2	3	4	5	6	7	8	9	10	11	12	13
<u>VD</u>	<u>SR</u>	<u>16M</u>	<u>08</u>	<u>X</u>	<u>S</u>	<u>44</u>	<u>X</u>	<u>X</u>	<u>4</u>	<u>C</u>	<u>12</u>	-
VDIC												
SRAM												
Capability: 16Mbit												
Bus Width: 8bit												
R= Radiation Data Tested; V= Generic Radiation Data Available												
Package: SOP												
Pin Quantity: 44 Pin												
Temperature: E=0~+70°C;I=-40~+85°C; M=-55~+125°C												
Quality: E= Sample; B= Industry; M=Military; S= Space												
Stacking Layer: 4layer												
Power Supply : 5.0V												
Speed: 12ns												
Version: First Version												

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (°C)
			TID ¹	SEL ²	SEU ³		
VDSR16M08VS44EE4V12	16M	8	-	-	-	SOP44	0 ~ + 70
VDSR16M08VS44IB4V12	16M	8	-	-	-	SOP44	-40 ~ + 85
VDSR16M08VS44MM4V12	16M	8	-	-	-	SOP44	-55 ~ + 125
VDSR16M08RS44MS4V12	4M	8	> 100	> 59	> 0.2	SOP44	-55 ~ + 125

¹ TID: Total Dose (Krad(Si))

² SEL: LET Threshold (Mev.cm2/mg)

³ SEU:SEU Threshold (Mev.cm2/mg)

8 Package Dimensions

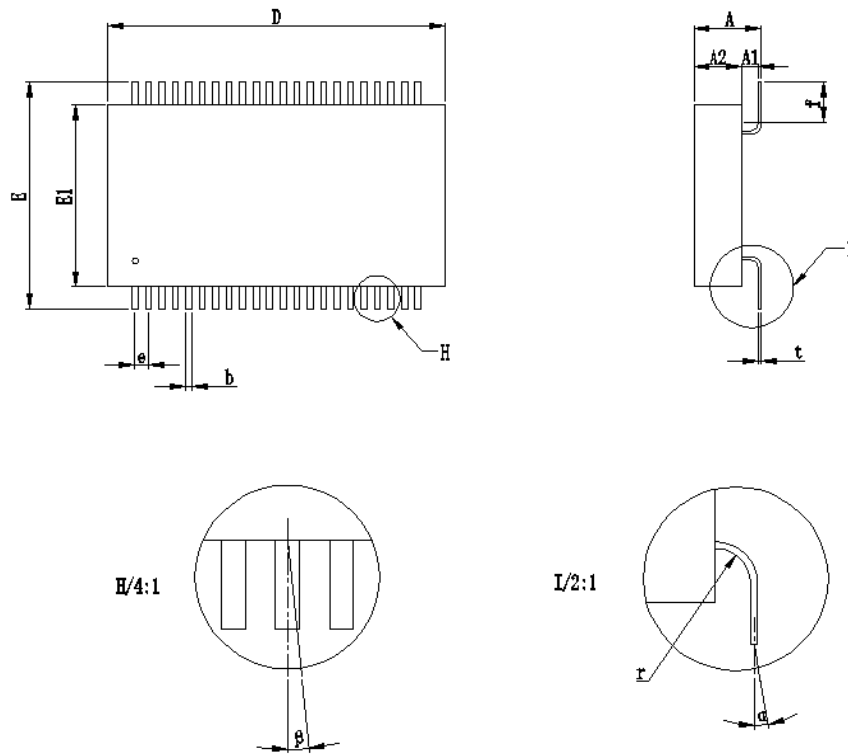


Figure 3 Package dimensions

Table 6 Dimensions information

	Min	Max
A	3.70	4.40
A2	2.50	3.10
D	19.80	20.20
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35	
e	0.80	
r	1.00	
t	0.20	
α	$\leq 3^\circ$	
β	$\leq 3^\circ$	

NOTE: 1. Unit: mm 2. A1= A - A2

9 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Oct 24,2018	First Created