

VDIC NOR FLASH MEMORY

VDRF512M16XS56XX8V90 USER MANUAL

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Contents

1	DESCRIPTION	1
2	FEATURES	1
3	BLOCK DIAGRAM	2
4	PIN DESCRIPTIONS– SOP-56.....	2
5	ELECTRICAL SPECIFICATIONS.....	4
	5.1. ABSOLUTE MAXIMUM RATINGS	4
	5.2. RECOMMENDED OPERATING RANGES	4
	5.3. DC Characteristics Tables.....	5
6	TYPICAL APPLICATION	5
7	ORDERING INFORMATION.....	5
8	PACKAGE DIMENSIONS	7
9	REVISION HISTORY	8

VDIC-NOR Flash Memory

HIGH-SPEED 3.3V 32M × 16bit

1. DESCRIPTION

The VDRF512M16XS56XX8V90 is a 512Mbit high-density simultaneous Read/Write FLASH Memory module organized as $8 \times 4M \times 16\text{bit}$.

Using high-performance and high-reliability technology chips, stacking with the well-known ORBITA Proprietary technology, this FLASH memory module provides a cost-effective solution for low power and high-capacity non-volatile memory data storage needs.

Each device of the module is a 64Mbit FLASH Memory, organized $4M \times 16\text{bit}$ that can be accessed by activating the associated control signals(#CE and #WP/ACC),and electrically erasable, read/write non-volatile flash memory. Any word can be programmed typically in $8\mu\text{s}$. The device features 3.3V voltage read and write operation, with access times as fast as 90ns to eliminate the need for WAIT states in high-performance microprocessor systems. This device is designed to allow either single Sector or full Chip erase operation, where each Sector can be individually protected against program erase operations or temporarily unprotected to erase or program. The device can sustain a minimum of 1 million program erase cycles on each Sector. The VDRF512M16XS56XX8V90 module is packaged in a 56 SOP package and is available for commercial, industrial and military temperature range.

2. FEATURES

- Single 3.3V power supply.
- Organization $32M \times 16\text{-Bit}$.
- Simultaneous Read/Write operation.
- Data can be continuously read one bank while executing erase/program functions in another bank.
- Zero latency between read and write operation.
- Flexible bank architecture.
- Boot sectors.
- Top and bottom boot sectors in the same device.
- Any combination of sectors can be erased.
- Zero power operation.
- Sophisticated power management circuits reduce power consumed during inactive periods to nearly zero.
- High performance
- Access time as fast as 90ns.
- Program time: $4\mu\text{s}/\text{word}$ typical utilizing accelerate function.
- Ultra low power consumption.
- Minimum 1 million erase cycles guaranteed per sector.
- 20 years data retention

3. BLOCK DIAGRAM

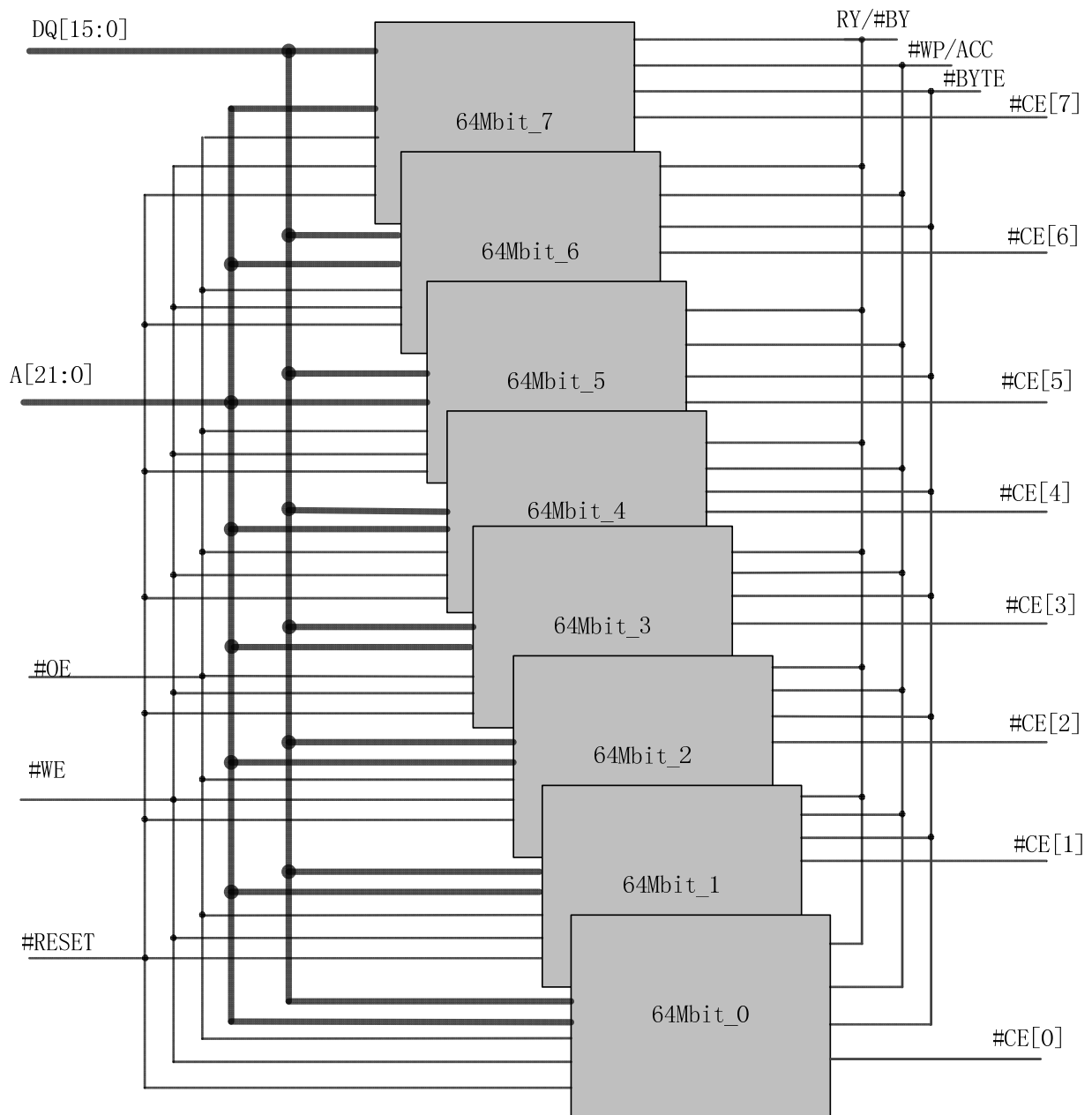


Figure 1 Block diagram

4. PIN DESCRIPTIONS– SOP-56

Pin Id	Pin #		Pin Id
NC	1	56	#CE7
#CE4	2	55	#CE1
A15	3	54	A16
A14	4	53	#BYTE
A13	5	52	VSS
A12	6	51	DQ15
A11	7	50	DQ7
A10	8	49	DQ14
A9	9	48	DQ6
A8	10	47	DQ13
A19	11	46	DQ5
A20	12	45	DQ12
#WE	13	44	DQ4
#RESET	14	43	VCC
A21	15	42	DQ11
#WP/ACC	16	41	DQ3
RY/#BY	17	40	DQ10
A18	18	39	DQ2
A17	19	38	DQ9
A7	20	37	DQ1
A6	21	36	DQ8
A5	22	35	DQ0
A4	23	34	#OE
A3	24	33	VSS
A2	25	32	#CE0
A1	26	31	A0
#CE3	27	30	#CE2
#CE5	28	29	#CE6

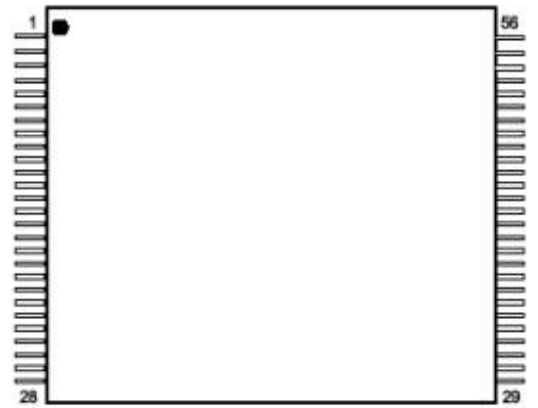


Figure 2 Pin configuration

Table 1 Pin description

Pin Name	Function
A0-A21	Address inputs
DQ0-DQ15	Data Inputs/Outputs
#CE [7:0]	Chip Enable
#OE	Output Enable
#WE	Write Enable
#WP/ACC	Write Protect / Acceleration Pin
#RESET	Hardware Reset Pin
#BYTE	Byte/Word mode selection
RY/#BY	Ready/Busy Output
Vcc	Supply Voltage(2.7-3.6V)
Vss	Ground
NC	Not Connected to anything

5. ELECTRICAL SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.5 ~ +4.0	V
Voltage on any pin relative to V _{SS}	V _{IN}	-0.5 ~ +4.0	V
Power Dissipation	P _D	1.0	W
Operating Temperature Range	T _{OPR}	-55 ~ +125	°C
Storage Temperature Range	T _{STG}	-65 ~ +150	°C

5.2 RECOMMENDED OPERATING RANGES

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.7	3.3	3.6	V
Input high voltage	V _{IH}	0.7×V _{CC}	—	V _{CC} +0.3	V

Parameter	Symbol	Min	Typ	Max	Unit
Input low voltage	V_{IL}	-0.5	—	0.8	V

5.3 DC Characteristics Tables

Table 4 DC characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	$V_{CC}=2.7V, I_{OL}=+4mA$	—	0.45	V
Output voltage high level	V_{OH}	$V_{CC}=2.7V, I_{OH}=-2mA$	2.3	—	V

6. TYPICAL APPLICATION

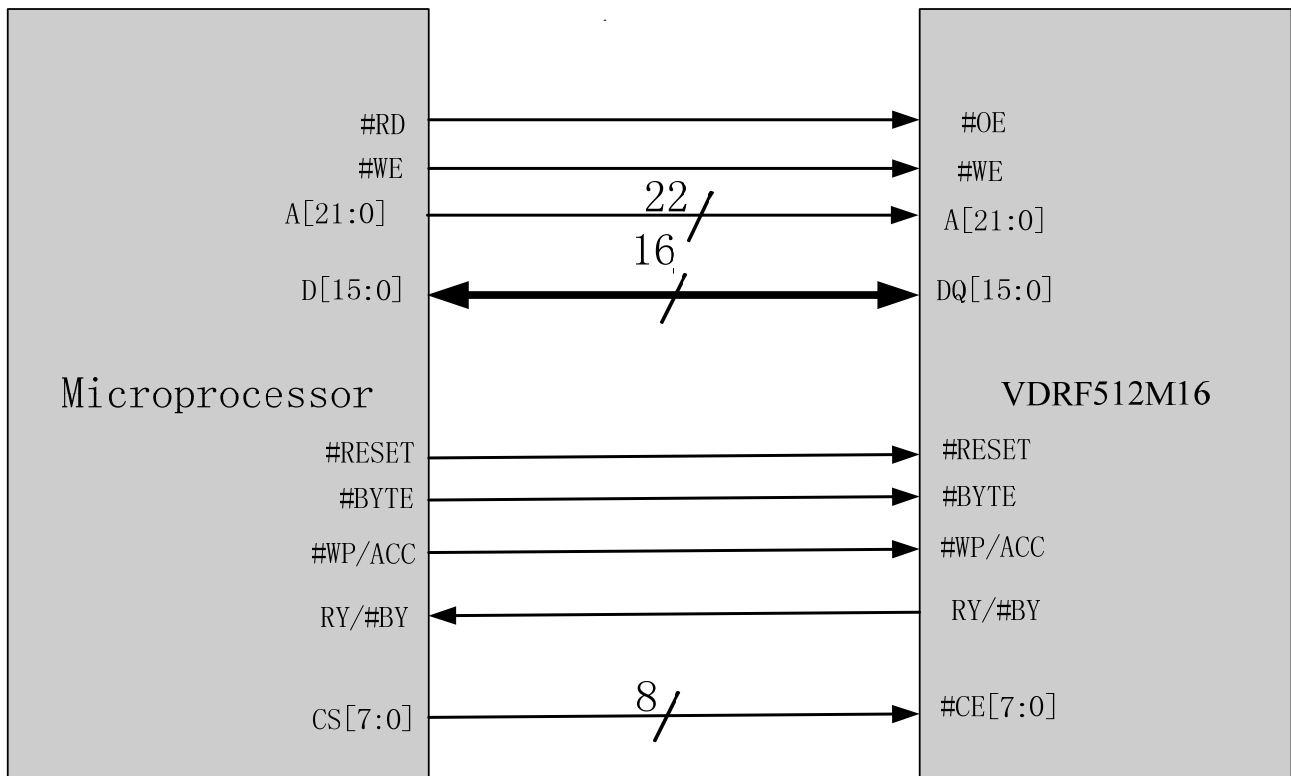


Figure 3 Typical application

7. ORDERING INFORMATION

1	2	3	4	5	6	7	8	9	10	11	12	13
<u>VD</u>	<u>RF</u>	<u>512M</u>	<u>16</u>	<u>X</u>	<u>S</u>	<u>56</u>	<u>X</u>	<u>X</u>	<u>8</u>	<u>V</u>	<u>90</u>	-
VDIC												
NOR FLASH												
Capability: 512M bit												
Bus Width: 16bit												
R= Radiation Data Tested; V= Generic Radiation Data Available												
Package: SOP												
Pin Quantity: 56 Pin												
Temperature: E=0~+70°C;I=-40~+85°C; M=-55~+125°C												
Quality: E= Sample; B= Industry; M=Military; S= Space												
Stacking Layer: 8layer												
Power Supply : 3.3V												
Speed: 90ns												
Version: First Version												

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (°C)
			TID ¹	SEL ²	SEU ³		
VDRF512M16VS56EE8V90	512M	16	-	-	-	SOP56	0~+70
VDRF512M16VS56IB8V90	512M	16	-	-	-	SOP56	-40~+85
VDRF512M16VS56MM8V90	512M	16	-	-	-	SOP56	-55~+125
VDRF512M16RS56MS8V90	512M	16	>15	>99.8	>4.7	SOP56	-55~+125

¹ TID: Total Dose (Krad(Si))

² SEL: LET Threshold (Mev.cm2/mg)

³ SEU:SEU Threshold (Mev.cm2/mg)

8. PACKAGE DIMENSIONS

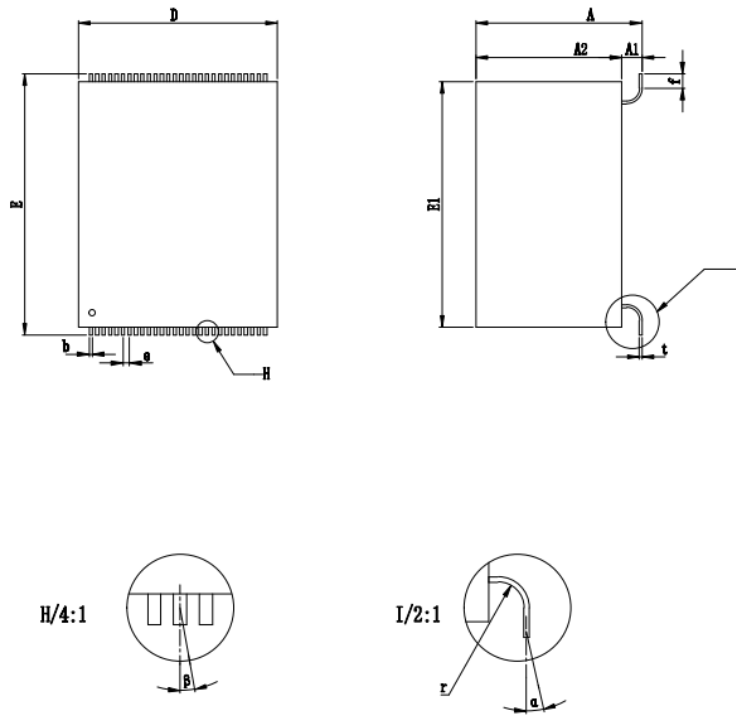


Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	12.30	12.80
A2	11.10	11.50
D	15.20	15.60
E	19.80	20.20
E1	18.80	19.20
f	1.00	1.40
b	0.22	0.28
e	0.50	
r	1.00	1.20
t	0.18	0.22
α	$\leq 3^\circ$	
β	$\leq 3^\circ$	
NOTE: 1. Unit: mm 2. $A1 = A - A2$		

9. REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	May 29,2018	First Created
A1	Jul 10,2019	Change PACKAGE DIMENSIONS
B0	Mar 21,2020	Update TID and SEE